WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor power device, comprising:

identifying an active region on a semiconductor die;

identifying a first region in said active region;

identifying a second region in said active region;

providing a first cell design by which active cells in said first region will be fabricated; and

providing a second cell design by which active cells in said second region will be fabricated,

said first cell design being different from said second cell design.

2. The method of claim 1 wherein said first cell design and said second cell design include cell dimensions such that a cell density of said first region is different from that of said second region.

3. The method of claim 1 wherein said first cell design includes at least one physical dimension different from that included in said second cell design.

4. The method of claim 3 wherein said physical dimension includes a channel width.

5. The method of claim 4 wherein said physical dimension includes a cell die area.

6. The method of claim 1 wherein said first cell design includes a material composition for cells that is different from that of said second cell design.

7. The method of claim 1 wherein said first cell design differs from said second cell design with respect to current density.

8. The method of claim 1 wherein said first cell design differs from said second cell design with respect to source resistance.

9. The method of claim 1 wherein said first cell design differs from said second cell design with respect to transconductance.

10. The method of claim 1 wherein said first cell design differs from said second cell design with respect to gain.

11. The method of claim 1 wherein said first cell design differs from said second cell design with respect to threshold voltage.

12. The method of claim 1 wherein said first cell design and said second cell design are field effect transistors.

13. The method of claim 1 wherein said first cell design and said second cell design are memory cells.